Atty. Docket No. 55123P268
Express Mail Label No. EV387143799US

UNITED STATES PATENT APPLICATION

FOR

MULTICHANNEL HIGH RESOLUTION SEGMENTED RESISTOR STRING DIGITAL-TO-ANALOG CONVERTERS

INVENTORS:
Simon Bevan Churchill
Gaurang Arvind Shah
David Webb
Bharath Mandyam

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(714) 557-3800

MULTICHANNEL HIGH RESOLUTION SEGMENTED RESISTOR STRING DIGITAL-TO-ANALOG CONVERTERS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of digital-to-analog converters (DACs)

2. Prior Art

Designing multiple-channel (such as greater than 8), high-resolution DACs (such as greater than 14-bits) in minimum die area has always been a challenging problem in the analog world. In many level-setting and closed loop applications, multiple high-resolution DAC channels are required that need guaranteed monotonic behavior and better than 12-bits of absolute accuracy.

Normally, R-2R DACs are used for high resolution and accuracy. The resolution of an untrimmed R-2R DAC is limited to 10 to 12-bits. In order to guarantee differential nonlinearity (DNL) at greater than a 14-bit level, a significant amount of trimming is involved, which in turn adds substantial cost to the integrated circuit. Also since the input resistance looking into the DACs is relatively smaller for multi channel DACs, precision buffers are needed

for the high and low references for such architecture. Precision buffers are expensive in terms of die area.

Integrating multiple channels of independent high-resolution DACs also contributes to significant die-area that adds both to the cost and the footprint of the integrated circuit. Sample and hold approaches have been proposed that cut down the die-area for a multi-channel, high resolution DAC, but this generally results in pedestal, droop and feedthrough errors owing to the sampling nature of the system.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a simplified diagram illustrating the architecture of an exemplary N-bit DAC in accordance with the present invention.

Figure 2 is a diagram illustrating multiple channels (secondary or B resistor strings and tertiary or C resistor strings and associated circuitry) operative from the single primary or A resistor string.

Figure 3 presents an exemplary circuit for generating replica currents.

Figure 4 is a diagram illustrating one channel of an M channel DAC, including interconnections for leapfrogging.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention uses a novel architecture for multichannel DACs that achieves guaranteed monotonicity, high-channel density (M-channels of N-bit DAC) and good accuracy (integral nonlinearity, or INL) over the prior art at a significantly lower die area and trim cost. The architecture is based on 3-stage resistor string segmentation. It is comprised of an "A"-bit primary string that is shared between M lower-order DACs. Each lower order DAC comprises of "B"-bit secondary string and "C"-bit tertiary string. Low impedance buffers and replica biased bootstrapped current sources at the output of the common primary string taps allow sharing of the "A" MSB bits between all of the M DACs.

The unique architecture divides the effective resolution and accuracy into "A" MSB bits of primary and "B + C" bits of secondary DACs. The "A" bits of MSBs, being shared between pluralities of secondary DACs, reduce the die area significantly. The buffers that are needed for R-2R DACs are used as a means to buffer the primary string outputs, thereby offering low impedance reference levels that the secondary DACs interpolate between to give the final output. Hence the architecture is extremely compact and efficient for multi-channel, high resolution DACs.

Figure 1 is a simplified diagram illustrating the architecture of an exemplary N-bit DAC in accordance with the present invention. A primary 2^A element resistor string implements the "A" MSBs. Each tap of the primary string is buffered, effectively splitting the reference voltage into $(2^A + 1)$ low-impedance voltage levels (including V_{REF} and GND) or 2^A voltage increments that can then be shared by the M-channel lower order DACs, where each voltage increment is equal to $V_{REF}/2^A$.

There are two sources of mismatch in the "A" MSB string, which are the chief contributors to INL. Resistor mismatch induced INL will peak at mid-code without the trimming of any of the 2^A resistors. In order to reduce this error and to minimize the number of trim resistors, "D" bit (where "D" is less than "A") laser trimmed resistors are preferably placed in parallel with the primary string. The "D" bits are the most significant of the A most significant bits (MSBs). By precisely trimming the "D" bit resistors to $(\frac{1}{2})^D$, $(\frac{1}{2})^{(D-1)}$....$(2^D-1)/(2^D)$ of the reference voltage, the INL error due to resistor mismatch is reduced by $\frac{1}{2}^{(D/2)}$ of the peak value.

The buffered outputs of the D bits are coupled to corresponding A bit output switches, and to multiple (2^D) 2^{A-D} resistor strings, the nodes of which are buffered and coupled

to respective A bit output switches for the total of $(2^A + 1)$ A bit output voltages, including the ground GND and V_{REF} voltages.

Alternatively, the D bit strings may be eliminated and the A bit string trimmed, as each A bit node is buffered and thus not disturbed by loading. As a further alternative, D may equal A, in which case the D bit string entirely does away with the 2^{A-D} resistor strings between the D bit string nodes. However using a value of D greater than zero and less than A is preferred as providing a preferred combination of ease of trimming and desired performance.

Each of the nodes in the primary string have buffers that include a fast integrator and current sensing output stage that gives a wideband low impedance output to minimize the coupling between the lower order DACs during code switching. The offset of these buffers is the other large source of INL error. The buffers are designed with a low offset and drift input stage. In addition, as subsequently described in greater detail, a novel post-package trim scheme is integrated with these amplifiers that allows for package level trimming of the initial offset and temperature drift. Die-attach and point stresses caused by packages contribute to large shifts in offsets of active circuits. Hence, by trimming the buffers after packaging, extremely small levels

of offsets are achieved, giving excellent INL performance. Since these "A" bits are the MSBs and common to all M DACs, they could be the largest contributor to nonlinearity of each "N" bit DAC. An additional advantage of common "A" MSBs is consistent INL performance over all the "M" channels.

The next "B" bits are independent for each DAC and are each implemented as a 2^B element resistor string (secondary ladder) that interpolates between any two adjacent primary (A bit) levels via a pair of CMOS transmission gates. Figure 1 illustrates an interconnect circuit AB INT coupling a B resistor string of 2^B resistors to the A resistor string, and an interconnect circuit BC INT coupling a C resistor or tertiary string of 2^C resistors to the B resistor string, with an output select set of switches OUT SEL selecting the appropriate C resistor string node voltage as the DAC OUT output. The interconnect circuit AB INT, the B resistor string, the interconnect circuit BC INT and the output select switches OUT SEL are replicated for the rest of the M channels of the multiple channel DAC.

Leapfrogging (moving one end of the ladder at a time for each increment) is preferably, but not necessarily employed to transition between consecutive primary (A string) levels to reduce the number of CMOS transmission gates. Using leapfrogging, one end of each B resistor string need only be

connectable to the odd numbered outputs of the A string (GND or first output, third, fifth, .., V_{REF}), and the other end connectable to the even numbered outputs of the A string (second, fourth, etc). This is illustrated in Figure 4, wherein in the AB INT circuit, every other A string switch output is connected to one B string input. Thus, the number of CMOS switches needed (with leapfrogging) and for all M channels is:

$$\text{number of switches} = (2^A + 1)*M \qquad \text{Equation 1}$$

This is to be compared with the number of switches needed if one end of each B resistor string had to be connectable to all nodes except V_{REF} and the other end had to be connectable to all nodes of the B resistor string except GND, which would require (without leapfrogging):

$$\text{number of CMOS switches} = 2^{(A+1)}*M \qquad \text{Equation 2}$$

Using leapfrogging, closing any two adjacent AB INT switches couples the voltage between each adjacent pair of A string outputs ($V_{REF}/2^A$) across the B bit resistor string. However, using leapfrogging, the A string output reverses polarity on each incremental change of the A string output (hence the +/- and -/+ indications in Figure 4).

A pair of replica-biased current sources associated with each of the B resistor strings (M total) avoid current loading due to the secondary (B) string and effectively bootstraps the secondary string resistance. This current is switched into the secondary resistor string ends so that the primary buffers nominally do not need to provide any current. Without the replica-based bootstrap current, the voltage drop across the CMOS transmission gates (the switches in the AB INT circuit of Figures 1 and 4) and the metal track resistance would cause a positive DNL error at the primary code transitions.

An exemplary circuit for generating the replica currents is shown in Figure 3. The object of the circuit is to mirror equal positive (I_{UP}) and negative (I_{DN}) currents to each B resistor string, each of a magnitude to cause a nominal voltage drop across the resistor string equal to the voltage increment between adjacent primary string outputs. Thus the value of each bootstrap current is:

$$I_{UP} = I_{DN} = V_{REF}/2^{A}*2^{B}*R_{S}) \qquad \text{Equation 3}$$

where: R_S is the unit resistor in the secondary ladder

Again, "M" pairs of replica-currents are needed to support the independent lower order DACs. In Figure 3, amplifier A controls transistor Q1 so that the voltage across the resistor having a value equal to the total resistance of

each B resistor string ($2^B * R_S$, where R_S is the value of each resistor in each B string) is equal to the voltage between each adjacent pair of A string outputs ($V_{REF}/2^A$). That current is mirrored by transistor Q2 to M transistors Q30 through Q3(M-1) to provide the M positive currents I_{UP}. That current is also mirrored by transistors Q3 and Q4 to M transistors Q40 through Q4(M-1) to provide the M negative currents I_{DN}. In one embodiment, these current sources incorporate resistor trimming for enhanced current matching.

As stated before, the use of leapfrogging causes the polarity of the A string output to reverse on each incremental change in the A string output. To accommodate this, the current sources I_{UP} and I_{DN} must be connected to each respective B string with the proper polarity for the then existing A string output. Thus, as shown in Figure 4, switches are provided to couple either current sources I_{UP} or I_{DN} to each end of each B bit resistor string for this purpose (see the indication of bi-directional current sources I_{UP}/I_{DN} and I_{DN}/I_{UP} in Figure 1).

The last "C" bits of each channel are implemented as a 2^C element resistor or tertiary string that interpolates between consecutive secondary string voltage levels. By choosing the resistance R_S of individual resistors in the B

bit resistor string and the resistance R_T of individual resistors in the C bit resistor string such that $R_T >> R_S$, the loading error due to the tertiary or C bit ladder may be reduced. Since the last "C" bits form LSBs for the overall DAC, by properly choosing the ratio between R_T and R_S, an acceptably small DNL error for the overall N bit DAC can be achieved. In a preferred embodiment, leapfrogging is used for the coupling of the C bit resistor string to the output of the B bit resistor string, again minimizing the number of switches needed in the BC INT circuit. However, while leapfrogging is used for both A string switching to the B strings and B string switching to the respective C string, leapfrogging may be used in one but not the other, or not used at all, as desired.

The LSB of the overall N bit DAC is given by:

$$LSB = V_{REF}/(2^{(A+B+C)}); \text{ where } N = A + B + C \qquad \text{Equation 4}$$

In Figures 1 and 4, only one channel is specifically illustrated in order to allow the illustration of more detail for a representative channel. In Figure 2, multiple channels (secondary or B resistor strings and tertiary or C resistor strings and associated circuitry) are illustrated. For each A resistor string buffered output, switches 0 through M - 1 (Figure 4) are provided in the AB INT circuitry (see Figure 1) to allow the selective coupling of that A resistor string

output increment ($V_{REF}/2^A$), or to assist in the coupling of an adjacent increment, to a respective one of the B bit resistor strings for each of the M channels of the DAC.

With the segmented architecture of the present invention, one can achieve guaranteed monotonicity, and with the combination of circuit techniques and package level trimming, multi-channel high resolution DACs can be realized at low cost. In that regard, as mentioned before, a novel post-package trim scheme is integrated with these amplifiers that allows for package level trimming of the initial offset and temperature drift, in a preferred embodiment, using fuse trims. In particular, after packaging trim capabilities are provided by a serial interface coupled to on-chip digital-to-analog converters (DACs) associated with the buffers, which allow trimming of the initial offsets and temperature drift. Hence, extremely small levels of offsets are achieved, giving excellent INL performance.

While certain preferred embodiments of the present invention have been disclosed herein, such disclosure is only for purposes of understanding the exemplary embodiments and not by way of limitation of the invention. It will be obvious to those skilled in the art that various changes in form and detail may be made in the invention without

departing from the spirit and scope of the invention as set out in the full scope of the following claims.